**What is claimed is:**

1. A semiconductor apparatus comprising:

a semiconductor device to be mounted on a circuit board;

a plurality of conductive posts electrically connected to the semiconductor device; and

a plurality of conductive bumps each provided on an outer end of each of the conductive posts, so that the plurality of conductive bump is soldered onto the circuit board when the semiconductor device is mounted on the circuit board, wherein

a distance between a peripheral edge of the semiconductor device and an outer edge of the conductive post is determined to be narrow so that a solderbility or wetting condition of the conductive bumps can be visibly recognized easily.

2. A semiconductor apparatus according to claim 1, wherein the distance is in a range between 50 to 100 micrometers.

3. A semiconductor apparatus according to claim 1, wherein the semiconductor device is provided with a plurality of electrode pads connected to the conductive posts, the electrode pads being arranged on a line extending the center of the semiconductor device.

4. A semiconductor apparatus according to claim 1, wherein the semiconductor device is provided with a plurality of electrode pads connected to the conductive posts, each of the electrode pads being arranged between two adjacent conductive posts.

5. A semiconductor apparatus according to claim 1, wherein the semiconductor device is provided with a plurality of electrode pads connected to the conductive posts, each of the electrode pads being arranged directly under a corresponding conductive post.

6. A semiconductor apparatus according to claim 1, wherein the conductive bumps are of solder.

7. A semiconductor apparatus comprising:

a semiconductor device to be mounted on a circuit board;

a plurality of conductive posts electrically connected to the semiconductor device;

a plurality of conductive bumps each provided on an outer end of each of the conductive posts, so that the plurality of conductive bumps are soldered onto the circuit board when the semiconductor device is mounted on the circuit board; and

a molding resin which covers a surface of the semiconductor device, wherein

the molding resin is shaped to have a step at a peripheral

edge of the semiconductor device entirely, the step having upper and lower level portions.

8. A semiconductor apparatus according to claim 7, wherein the difference in level between the upper portion and lower portion of the step is half of a thickness of the mold resin.

9. A semiconductor apparatus according to claim 7, wherein the difference in level between the upper portion and lower portion of the step is in a range between 40 to 60 micrometers.

10. A semiconductor apparatus according to claim 7, wherein the conductive bumps are of solder.

11. A semiconductor apparatus comprising:

a semiconductor device to be mounted on a circuit board;

a plurality of conductive posts electrically connected to the semiconductor device;

a plurality of first conductive bumps each provided on an outer end of each of the conductive posts, so that the plurality of first conductive bumps are soldered onto the circuit board when the semiconductor device is mounted on the circuit board;

a molding resin which covers a surface of the semiconductor device; and

an insulating layer which is formed at portions corresponding to the conductive posts and at a peripheral portion of the semiconductor device, wherein

the molding resin is shaped to have a peripheral side surface that is on the identical plane with a peripheral side surface of the semiconductor device.

12. A semiconductor apparatus according to claim 11, wherein

the insulating layer is formed to have a width of 100 to 200 $\mu$m.

13. A semiconductor apparatus according to claim 11, further comprising

a plurality of second conductive bumps each provided on the peripheral side surface of the conductive posts.

14. A semiconductor apparatus according to claim 11, wherein

the conductive bumps are of solder.

15. A method for fabricating a semiconductor apparatus according to claim 7, comprising the steps of:

providing a semiconductor wafer on which a plurality of

semiconductor devices are formed, each of the semiconductor device having electrode pads thereon;

providing a plurality of conductive post connected to the electrode pads of the semiconductor devices;

molding the semiconductor devices with a molding resin so that an upper surface of the molding resin is on the same plane with upper surfaces of the conductive posts;

removing a part of the molding resin to be located at a peripheral edge so that the peripheral edge of the molding resin has a step, the step having upper and lower level portions;

providing conductive bumps on outer ends of the conductive posts; and

dicing the semiconductor wafer to form a plurality of individual semiconductor apparatus.

16. A method according to claim 15, wherein

the difference in level between the upper portion and lower portion of the step is half of a thickness of the mold resin.

17. A method according to claim 15, wherein

the difference in level between the upper portion and lower portion of the step is in a range between 40 to 60 micrometers.

18. A method according to claim 15, wherein

the conductive bumps are of solder.

19. A method for fabricating a semiconductor apparatus according to claim 11, comprising the steps of:

providing a semiconductor wafer on which a plurality of semiconductor devices are formed, each of the semiconductor device having electrode pads thereon;

forming grooves at portions corresponding to dicing lines of the semiconductor wafer;

forming an insulating layer on the wafer so that the grooves are filled with the insulating layer but a part of the electrode pad of the semiconductor devices is not covered with the insulating layer;

forming a metal layer on the insulating layer and the part of the electrode pads, which is not covered with the insulating layer;

forming a rewiring layer on the metal layer;

providing a conductive post material that extend across each of the grooves;

molding the semiconductor wafer with a molding resin so that an upper surface of the molding resin is on the same plane with upper surfaces of the conductive post material;

providing a conductive bump material on each of the conductive post material; and

dicing the semiconductor wafer at the grooves to form a plurality of individual semiconductor apparatus.

20. A method according to claim 19, further comprising the steps of:

expanding the distance between two adjacent semiconductor devices after the dicing process; and

reflowing the distanced semiconductor devices so as to form a conductive soldering bump on a peripheral side surface of each of the conductive posts.

21. A method according to claim 19, wherein

the insulating layer is formed to have a width of 100 to 200 $\mu$m.

22. A method according to claim 19, wherein

the conductive bumps are of solder.